Amendment to the Claims:

Claim 1 (Previously Amended):

1. A method for forming a flash memory device in a semiconductor assembly, comprising the steps of:

forming a series of floating gate devices having their source electrodes connected together by a conductive implant into a defined active area, each source electrode being self-aligned to a respective gate electrode;

forming a metal interconnect running a major length of said connected together source electrodes, said metal interconnect making a substantially continuous contact therebetween and spanning completely between neighboring gate electrodes; and

forming a metal drain plug for each floating gate device of said series of floating gate devices, said metal drain plug connecting between a drain electrode of each said floating gate device and a digit line.

Claim 2 (Original):

2. The method of claim 1, wherein said step of forming a metal drain plug further comprises self-aligning said metal drain plug to a respective drain electrode.

Claim 3 (Previously Amended):

3. A method for forming a flash memory device on a semiconductor assembly comprising forming a metal interconnect running a major length of a series of source electrodes

connected together by a conductively doped active area, said source electrodes formed in a self-aligning manner to their respective gate electrodes, said metal interconnect having a majority of a bottom surface making contact to said conductively doped active area and spanning completely between neighboring gate electrodes.

Claim 4 (Previously Amended):

4. A method for forming a flash memory device on a semiconductor assembly comprising the steps of:

forming a series of floating gate devices having their source electrodes connected together by a conductively doped active area, said source electrodes being self-aligned to their respective transistor gates of each said floating gate device;

forming a nitride barrier layer overlying each transistor gate;

forming a planarized insulation layer over said nitride barrier layer;

removing portions of said planarized insulation layer while using said nitride barrier layer to self-align an interconnect via to said source electrodes;

forming a metal interconnect into said interconnect via, said metal interconnect running a major length of said connected together source electrodes and making contact therebetween and spanning completely between neighboring gate electrodes; and

forming a metal drain plug for each floating gate device of said series of floating gate devices, said metal drain plug self-aligned to and connected between a drain electrode of each said floating gate device and a digit line.

Claim 5 (Previously Amended):

5. A method for forming a flash memory device in a semiconductor assembly, comprising the steps of:

forming a series of floating gate devices having their source electrodes connected together by a conductive implant into a defined active area, each source electrode being self-aligned to a respective gate electrode;

forming a metal interconnect running a major length of said connected together source electrodes, said metal interconnect making a substantially continuous contact therebetween and spanning completely between neighboring gate electrodes; and

forming a metal drain plug for each floating gate device of said series of floating gate devices, said metal drain plug connecting between a drain electrode of each said floating gate device and a digit line.

Claim 6 (Original):

6. The method of claim 5, wherein said step of forming a metal drain plug further comprises self-aligning said metal drain plug to a respective drain electrode.

Claim 7 (Original):

7. A method for forming a flash memory device in a semiconductor assembly, comprising the steps of:

forming a series of floating gate devices having their source electrodes connected together by a conductive implant into a defined active area, each source electrode being self-aligned to a respective gate electrode;

forming a tungsten-based interconnect running a major length of said connected together source electrodes, said tungsten-based interconnect making a substantially continuous contact therebetween; and

forming a tungsten-based drain plug for each floating gate device of said series of floating gate devices, said tungsten-based drain plug connecting between a drain electrode of each said floating gate device and a digit line.

Claim 8 (Original):

8. The method of claim 7, wherein said step of forming a tungsten-based drain plug further comprises self-aligning said tungsten drain plug to a respective drain electrode.

Claim 9 (Original):

9. A method for forming a flash memory device on a semiconductor assembly comprising forming a tungsten-based interconnect running a major length of a series of source electrodes connected together by a conductively doped active area, said source electrodes formed in a self-aligning manner to their respective gate electrodes, said tungsten-based interconnect having a majority of a bottom surface making contact to said conductively doped active area.

Claim 10 (Original):

10. A method for forming a flash memory device on a semiconductor assembly comprising the steps of:

forming a series of floating gate devices having their source electrodes connected together by a conductively doped active area, said source electrodes being self-aligned to their respective transistor gates of each said floating gate device;

forming a nitride barrier layer overlying each transistor gate;

forming a planarized insulation layer over said nitride barrier layer;

removing portions of said planarized insulation layer while using said nitride barrier layer to self-align an interconnect via to said source electrodes;

forming a tungsten-based interconnect into said interconnect via, said tungsten-based interconnect running a major length of said source electrodes and making contact therebetween; and

forming a tungsten-based drain plug for each floating gate device of said series of floating gate devices, said tungsten-based drain plug self-aligned to and connected between a drain electrode of each said floating gate device and a digit line.

Claims 11-19 (Withdrawn):

11. A flash memory device comprising:

a series of floating gate devices each having an implanted source electrode self-aligned to a respective gate electrode, said implanted source electrodes being connected together by a conductively doped active area;

a metal interconnect running a major length of said connected together source electrodes, said metal interconnect making substantially continuous contact therebetween; and

a metal drain plug for each floating gate device of said series of floating gate devices, said metal drain plug connected between a drain electrode of each said floating gate device and a digit line.

12. The flash memory device of claim 11, wherein said metal drain plug is self-aligned to a respective drain electrode.

13. A flash memory device comprising:

a metal interconnect running a major length of a series of source electrodes self-aligned to their respective gate electrodes, said series of source electrodes being connected together by a conductively doped active area:

wherein a majority of a bottom surface of said metal interconnect makes contact to said conductively doped active area.

14. A flash memory device comprising:

a series of floating gate devices having their source electrodes connected together by a conductively doped active area, said source electrodes being self-aligned to their respective transistor gates of each said floating gate device;

a nitride barrier layer overlying each transistor gate;

a metal interconnect running a major length of said source electrodes being connected together and making contact therebetween; and

a metal drain plug for each floating gate device of said series of floating gate devices, said metal drain plug self-aligned to and connected between a drain electrode of each said floating gate device and a digit line.

15. A flash memory device comprising:

a series of floating gate devices each having an implanted source electrode self-aligned to a respective gate electrode, said implanted source electrodes connected together by a conductively doped active area;

a tungsten-based interconnect running a major length of said connected together source electrodes, said tungsten-based interconnect making substantially continuous contact therebetween; and

a tungsten-based drain plug for each floating gate device of said series of floating gate devices, said tungsten-based drain plug connected between a drain electrode of each said floating gate device and a digit line.

16. The flash memory device of claim 15, wherein said tungsten-based drain plug is self-aligned to a respective drain electrode.

17. The flash memory device of claim 15, wherein said tungsten-based interconnect and said tungsten-based drain plug is a metal selected from the group consisting of tungsten or tungsten/titanium.

18. A flash memory device comprising:

a tungsten-based interconnect running a major length of a series of source electrodes self-aligned to their respective gate electrodes, said series of source electrodes being connected together by a conductively doped active area:

wherein a majority of a bottom surface of said tungsten-based interconnect makes contact to said conductively doped active area.

19. The flash memory device of claim 18, wherein said tungsten-based interconnect is a metal selected from the group consisting of tungsten or tungsten/titanium.

Claim 20 (Previously Added):

20. A method for forming a flash memory device in a semiconductor assembly, comprising the steps of:

forming a series of floating gate devices having their source electrodes connected together by a conductive implant into a defined active area, each source electrode being self-aligned to a respective gate electrode;

forming a metal interconnect consisting of a metal nitride barrier layer and an overlying metal layer, said metal interconnect running a major length of said connected together source electrodes, said metal interconnect making a substantially continuous contact therebetween; and

forming a metal drain plug for each floating gate device of said series of floating gate devices, said metal drain plug connecting between a drain electrode of each said floating gate device and a digit line.